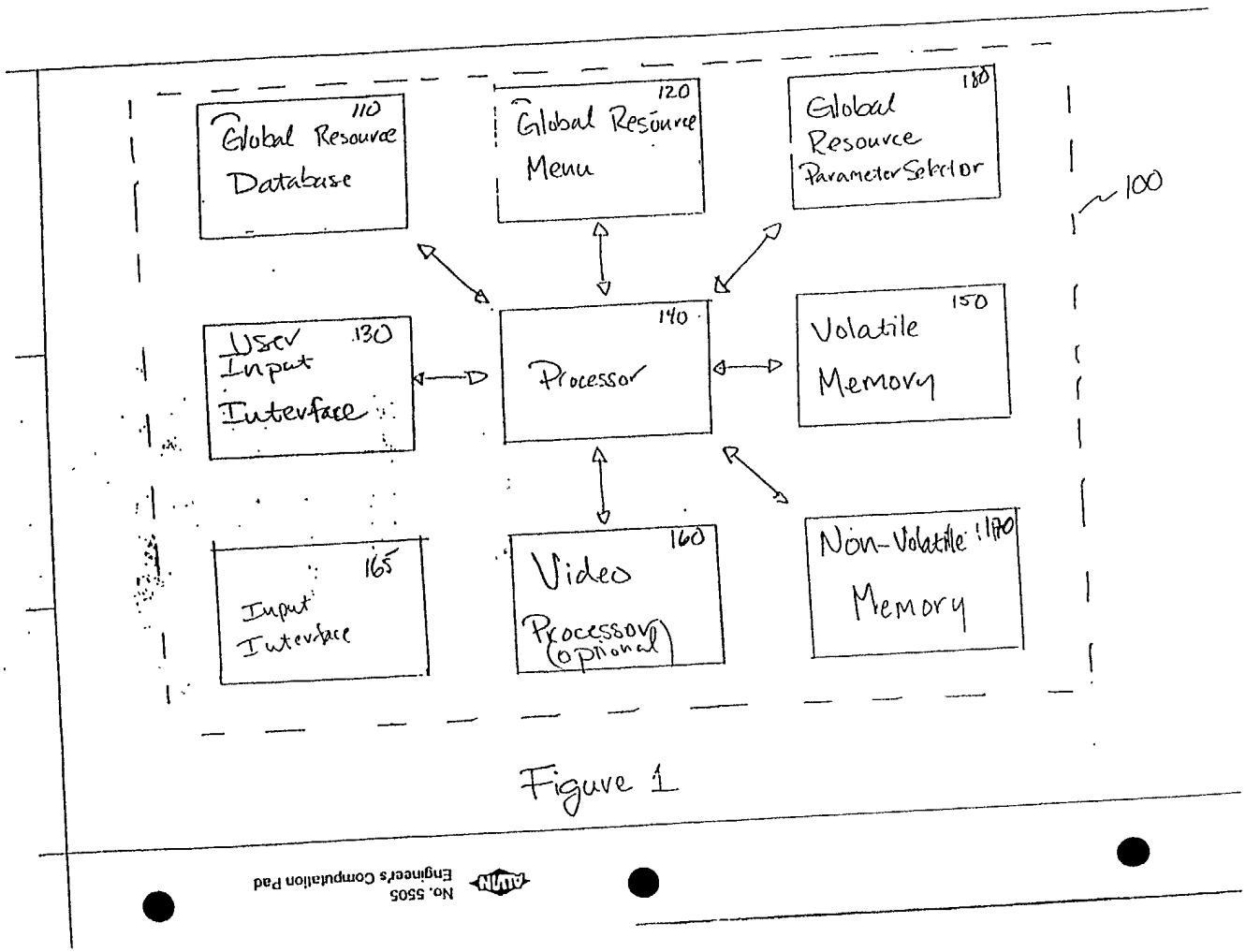


Figure 1

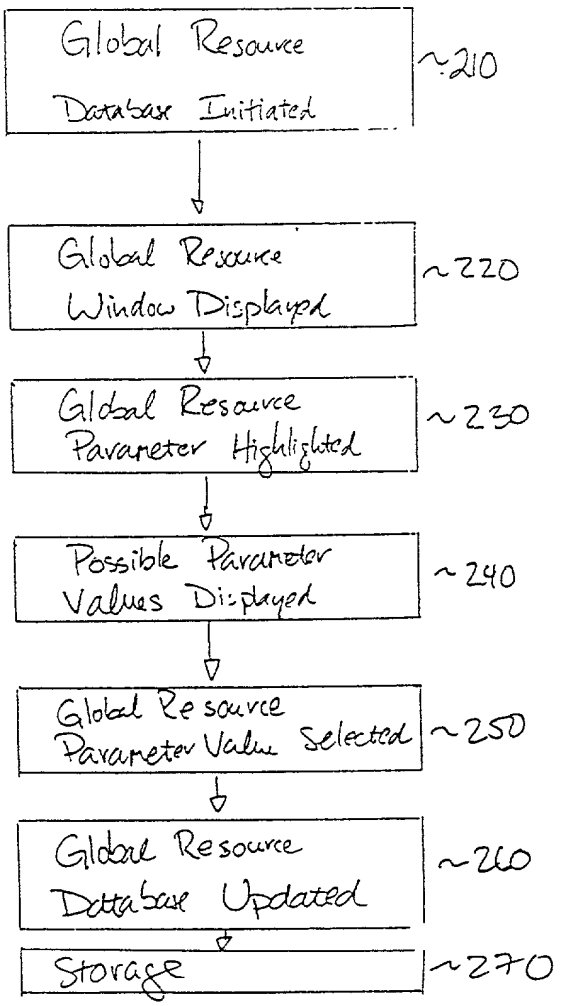


Figure 2A

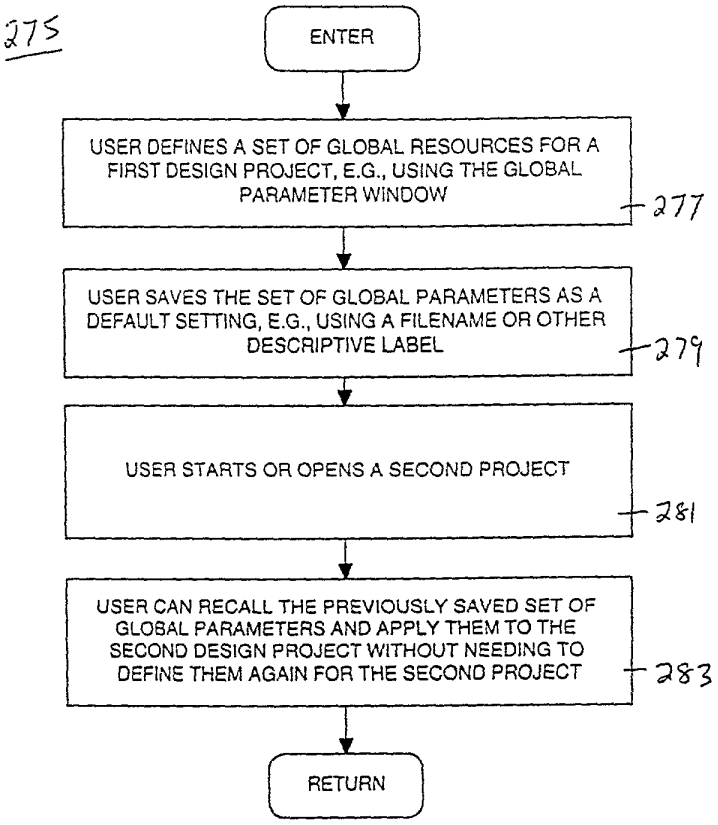

275
ENTER
USER DEFINES A SET OF GLOBAL RESOURCES FOR A FIRST DESIGN PROJECT, E.G., USING THE GLOBAL PARAMETER WINDOW
277
USER SAVES THE SET OF GLOBAL PARAMETERS AS A DEFAULT SETTING, E.G., USING A FILENAME OR OTHER DESCRIPTIVE LABEL
279
USER STARTS OR OPENS A SECOND PROJECT
281
USER CAN RECALL THE PREVIOUSLY SAVED SET OF GLOBAL PARAMETERS AND APPLY THEM TO THE SECOND DESIGN PROJECT WITHOUT NEEDING TO DEFINE THEM AGAIN FOR THE SECOND PROJECT
283
RETURN

FIG. 2B

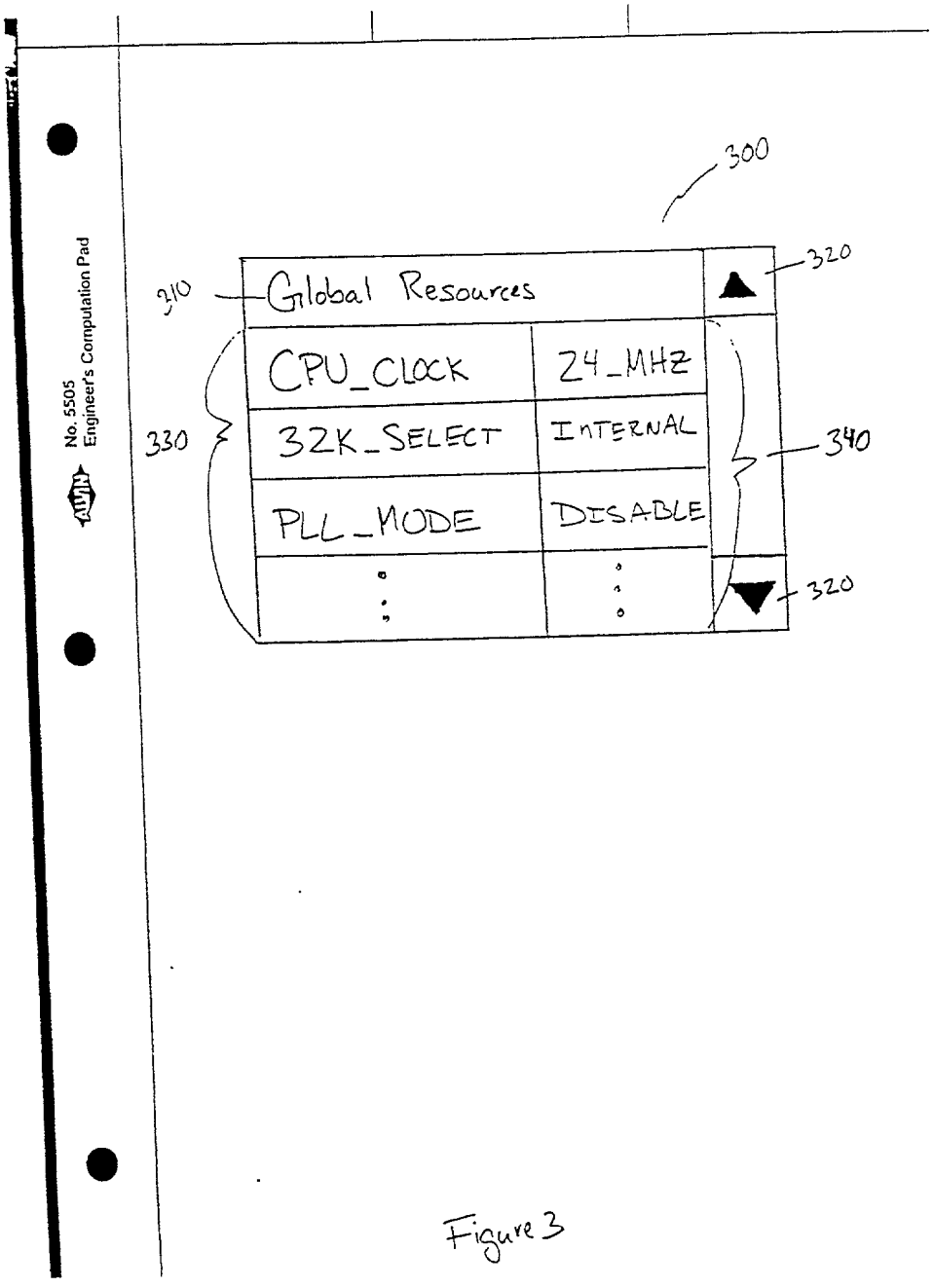

No. 5505
Engineer's Computation Pad
300
310
Global Resources
320
CPU_CLOCK
24_MHZ
32K_SELECT
INTERNAL
PLL_MODE
DISABLE
330
340
320

Figure 3

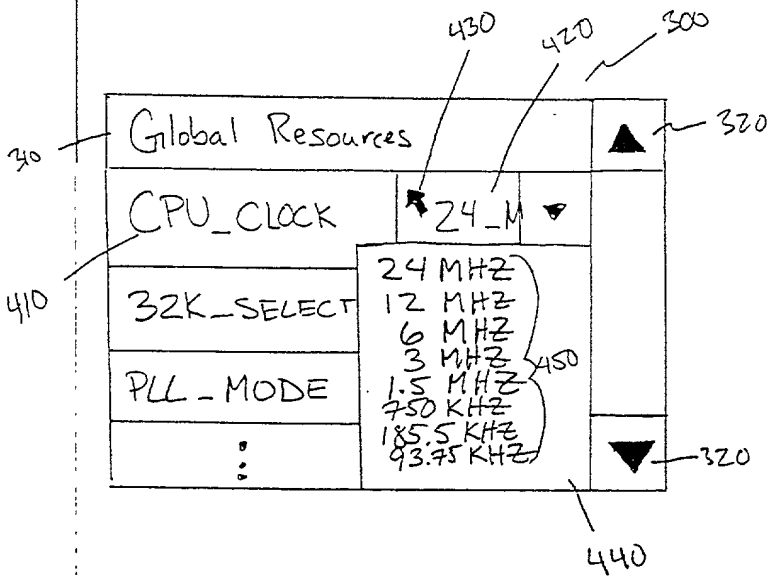

430
420
300
Global Resources
320
30
CPU_CLOCK
24_M
410
32K_SELECT
24 MHZ
12 MHZ
6 MHZ
3 MHZ
1.5 MHZ
750 KHZ
185.5 KHZ
93.75 KHZ
450
PLL_MODE
320
440

Figure 4

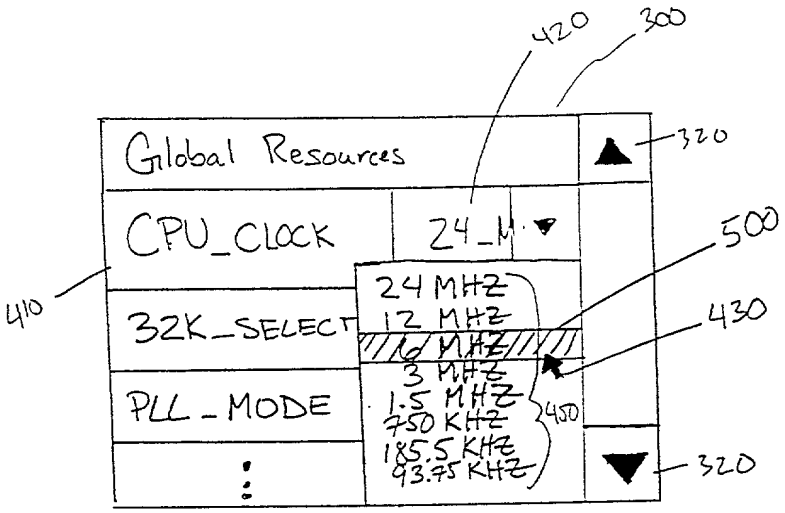
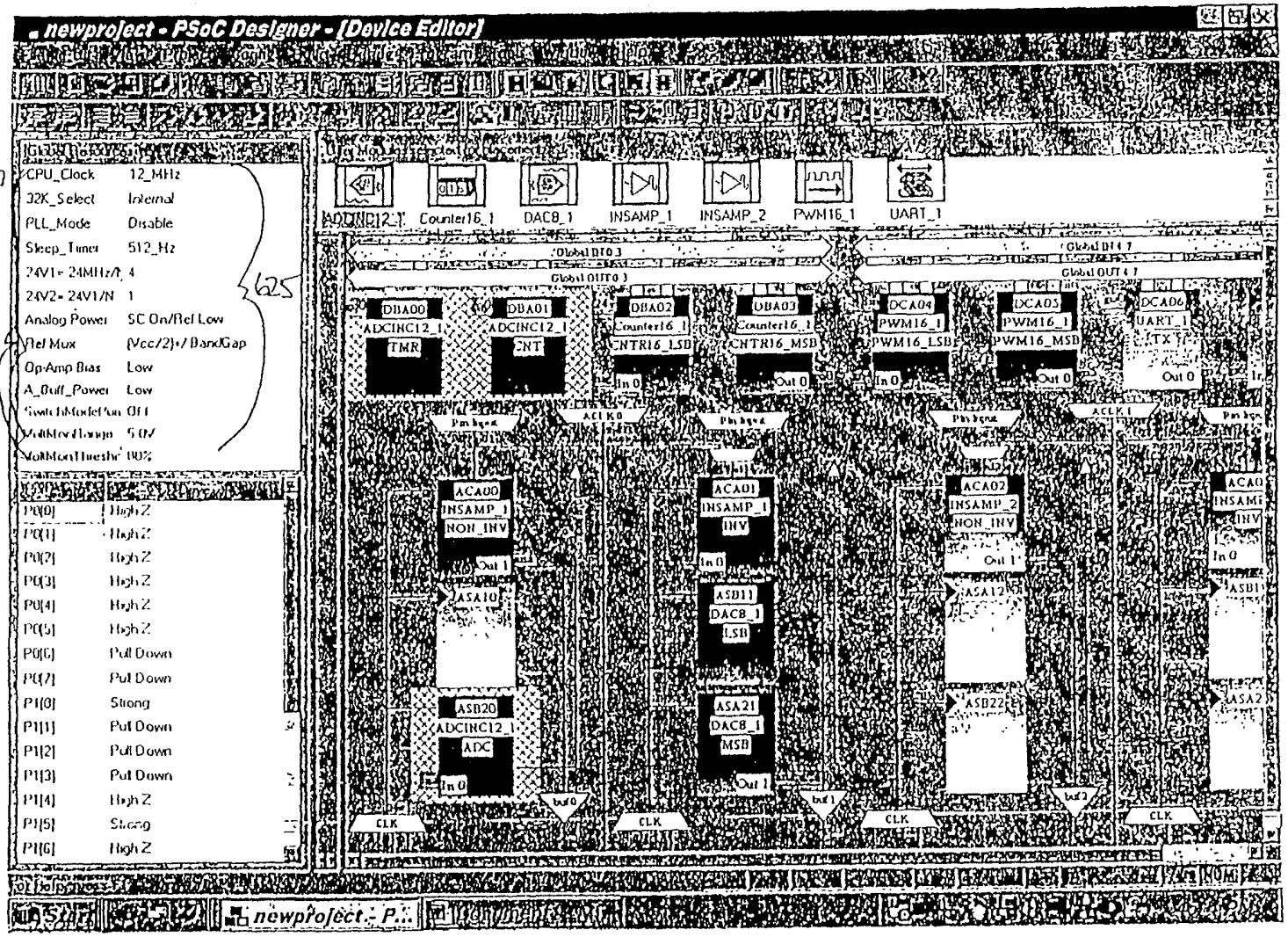
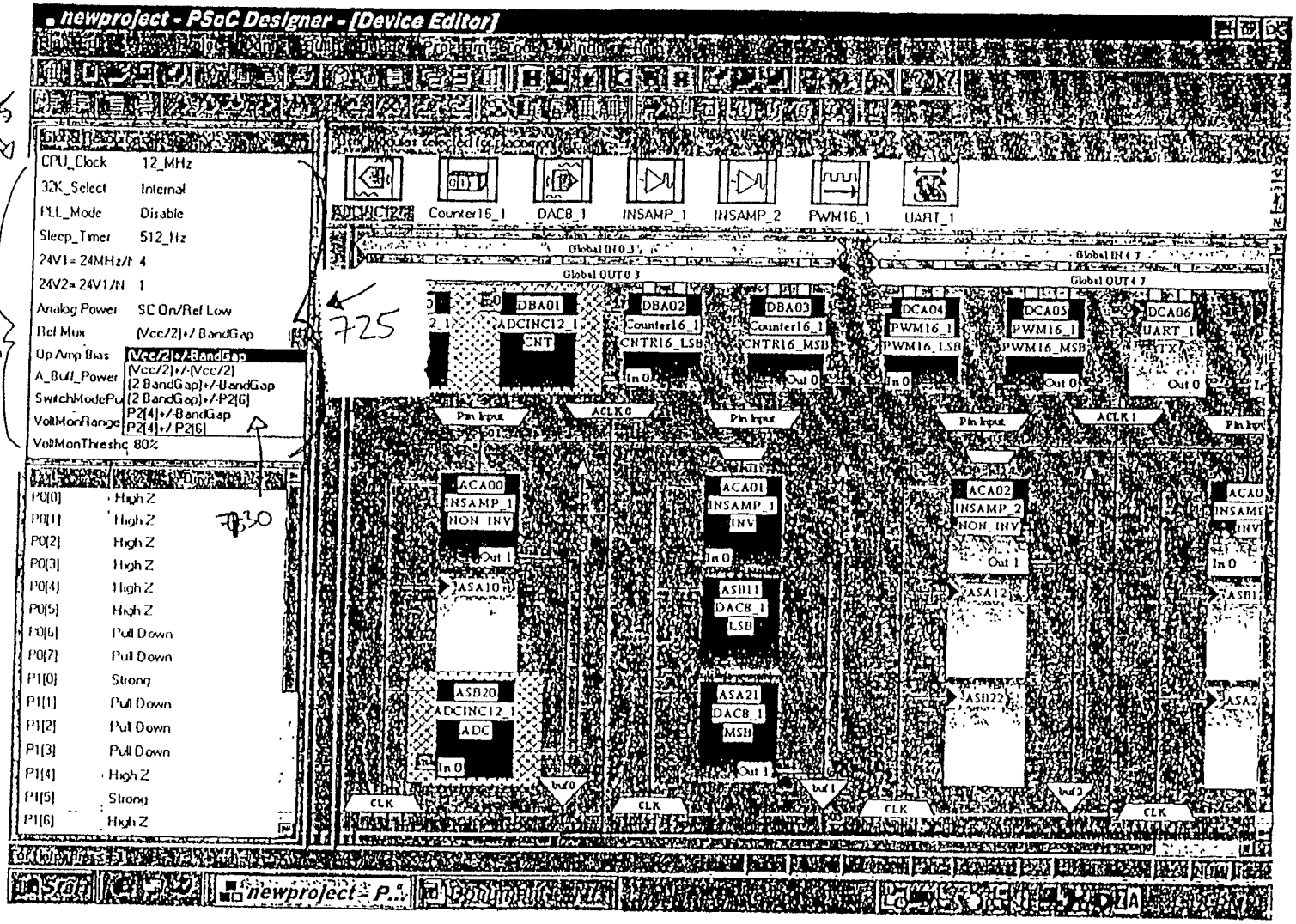

420
300
Global Resources
320
CPU_CLOCK
24_M
500
410
24 MHZ
12 MHZ
32K_SELECT
6 MHZ
430
3 MHZ
PLL_MODE
1.5 MHZ
750 KHZ
450
185.5 KHZ
93.75 KHZ
320

Figure 5


newproject - PSoC Designer - [Device Editor]
615
625
620
CPU_Clock 12_MHz
32K_Select Internal
PLL_Mode Disable
Sleep_Timer 512_Hz
24V1= 24MHz/1 4
24V2= 24V1/N 1
Analog Power SC On/Ref Low
Ref Mux (Vcc/2)+/-BandGap
Op-Amp Bias Low
A_Buff_Power Low
P0[0] High Z
P0[1] High Z
P0[2] High Z
P0[3] High Z
P0[4] High Z
P0[5] High Z
P0[6] Pull Down
P0[7] Pull Down
P1[0] Strong
P1[1] Pull Down
P1[2] Pull Down
P1[3] Pull Down
P1[4] High Z
P1[5] Strong
P1[6] High Z
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
DBA00
DBA01
DBA02
DBA03
DCA04
DCA05
DCA06
TMR
CNT
CNTR16_LSB
CNTR16_MSB
PWM16_LSB
PWM16_MSB
TX
ACA00
ACA01
ACA02
ACA0
NON_INV
INV
ASA10
ASB11
ASA12
ASB22
ASA21
ASA2
ASB20
ADC
LSB
MSB
In 0
Out 0
Out 1
CLK
buf0
buf1
buf2
start
newproject - P...

610

Fig. 6



710

Fig. 7